In the Claims:

Claims 1-7 (canceled).

Claim 8 (currently amended): A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a single gate insulating layer situated over an entire length of said third region and substantially less than an entire length of each of said first region and said second region, ~~the~~said single gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

a control gate situated over said single gate insulating layer.

Claim 9 (currently amended): A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; ~~and~~

a single gate insulating layer situated over an entire length of said third region and substantially less than an entire length of each of said first region and said second region, ~~the~~said single gate insulating layer having a first thickness situated over said first region

and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

an ONO stack situated over said single gate insulating layer.

Claims 10-13 (canceled).

Claim 14 (previously presented): A memory cell as in claim 8, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

Claim 15 (currently amended): A memory cell as in claim 8, wherein an injection field in an overlap region situated between said single gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

Claim 16 (currently amended): A memory cell as in claim 8, wherein an injection field in an overlap region situated between said single gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

Claim 17 (currently amended): A memory cell as in claim 8, wherein said single gate insulating layer comprises SiO_2.

Claim 18 (canceled).

Claim 19 (previously presented): A memory cell as in claim 9, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

Claim 20 (currently amended): A memory cell as in claim 9, wherein an injection field in an overlap region situated between said single gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

Claim 21 (currently amended): A memory cell as in claim 9, wherein an injection field in an overlap region situated between said single gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

Claim 22 (currently amended): A memory cell as in claim 9, wherein said single gate insulating layer comprises SiO_2.